IN THE CLAIMS

Please amend the claims as follows:

Claims 1-21 (Canceled).

Claim 22 (Previously Presented): A power semiconductor device, comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of the first conductivity type and a third semiconductor layer of a second conductivity type which are alternately and laterally arranged on the first semiconductor layer;

a first main electrode electrically in contact with the first semiconductor layer;

a fourth semiconductor layer of the second conductivity type selectively formed in surface regions of the second and third semiconductor layers;

a fifth semiconductor layer of the first conductivity type selectively formed in a surface region of the fourth semiconductor layer;

a second main electrode formed in contact with surfaces of the fourth and fifth semiconductor layers; and

a control electrode formed on surfaces of the second, fourth and fifth semiconductor layers,

wherein an impurity concentration of the first semiconductor layer is lower than that of the second semiconductor layer; and a layer thickness ratio A is given by an expression:

$0 < A = t / (t+d) \leqq 0.72$

where t is a thickness of the first semiconductor layer, and d is a thickness of the second semiconductor layer; and

wherein a void is present in a border region between the second semiconductor layer and the third semiconductor layer.

Claim 23 (Currently Amended): ~~The semiconductor device according to claim 21,~~ A power semiconductor device, comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of the first conductivity type and at least two third semiconductor layers of a second conductivity type which are alternately and laterally arranged on the first semiconductor layer;

a first main electrode electrically in contact with the first semiconductor layer;

a fourth semiconductor layer of the second conductivity type selectively formed in surface regions of the second and third semiconductor layers;

a fifth semiconductor layer of the first conductivity type selectively formed in a surface region of the fourth semiconductor layer;

a second main electrode formed in contact with surfaces of the fourth and fifth semiconductor layers; and

a control electrode formed on surfaces of the second, fourth and fifth semiconductor layers,

wherein an impurity concentration of the first semiconductor layer is lower than that of the second semiconductor layer; and a layer thickness ratio A is given by an expression:

$0 < A = t / (t+d) < 0.72$

where t is a thickness of the first semiconductor layer, and d is a thickness of the second semiconductor layer;

wherein insulating films are interposed between the second semiconductor layer and third semiconductor layers; and

wherein a void is present in said insulating films.

Claim 24 (Currently Amended): ~~A semiconductor device according to claim 21,~~ A power semiconductor device, comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of the first conductivity type and at least two third semiconductor layers of a second conductivity type which are alternately and laterally arranged on the first semiconductor layer;

a first main electrode electrically in contact with the first semiconductor layer;

a fourth semiconductor layer of the second conductivity type selectively formed in surface regions of the second and third semiconductor layers;

a fifth semiconductor layer of the first conductivity type selectively formed in a surface region of the fourth semiconductor layer;

a second main electrode formed in contact with surfaces of the fourth and fifth semiconductor layers; and

a control electrode formed on surfaces of the second, fourth and fifth semiconductor layers,

wherein an impurity concentration of the first semiconductor layer is lower than that of the second semiconductor layer; and a layer thickness ratio A is given by an expression:

$0 < A = t / (t+d) < 0.72$

where t is a thickness of the first semiconductor layer, and d is a thickness of the second semiconductor layer;

wherein insulating films are interposed between the second semiconductor layer and third semiconductor layers; and

wherein an impurity concentration profile of at least one of the second semiconductor layer and the at least two third semiconductor layers gradually reduces with depth.

Claim 25 (Previously Presented): A semiconductor device according to claim 23, wherein an impurity concentration profile of at least one of the second semiconductor layer and the at least two third semiconductor layers gradually reduces with depth.

Claim 26 (Previously Presented): A semiconductor device according to claim 22, wherein a plurality of voids are present independently along the border region.

Claim 27 (Previously Presented): A semiconductor device according to claim 22, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 28 (Previously Presented): A semiconductor device according to claim 23, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 29 (Previously Presented): A power semiconductor device, comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of the first conductivity type and a third semiconductor layer of a second conductivity type which are alternately and laterally arranged on the first semiconductor layer;

a first main electrode electrically in contact with the first semiconductor layer;

a fourth semiconductor layer of the second conductivity type selectively formed in surface regions of the second and third semiconductor layers;

a fifth semiconductor layer of the first conductivity type selectively formed in a surface region of the fourth semiconductor layer;

a second main electrode formed in contact with surfaces of the fourth and fifth semiconductor layers; and

a control electrode formed on surfaces of the second, fourth and fifth semiconductor layers,

wherein an impurity concentration of the first semiconductor layer is lower than that of the second semiconductor layer; and a layer thickness ratio A is given by an expression:

$0 < A = t/(t+d) \leqq 0.72$

where t is a thickness of the first semiconductor layer, and d is a thickness of the second semiconductor layer; and

wherein assuming that a breakdown voltage is represented by VB (V), then t, VB (V), and A satisfy a relationship below:

$t < 2.53 \times 10^{-6} \times (A \times VB)^{7/6}$ (cm),

wherein the first to fifth semiconductor layers are constituted by a silicon layer,

wherein a void is present in a border region between the second semiconductor layer and the third semiconductor layer, and

wherein a void is present in said insulating material.

Claim 30 (Previously Presented): A semiconductor device according to claim 29, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 31 (Previously Presented): A power semiconductor device, comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of the first conductivity type and a third semiconductor layer of a second conductivity type which are alternately and laterally arranged on the first semiconductor layer;

a first main electrode electrically in contact with the first semiconductor layer;

a fourth semiconductor layer of the second conductivity type selectively formed in surface regions of the second and third semiconductor layers;

a fifth semiconductor layer of the first conductivity type selectively formed in a surface region of the fourth semiconductor layer;

a second main electrode formed in contact with surfaces of the fourth and fifth semiconductor layers; and

a control electrode formed on surfaces of the second, fourth and fifth semiconductor layers,

wherein an impurity concentration of the first semiconductor layer is lower than that of the second semiconductor layer; and a layer thickness ratio A is given by an expression:

$0 < A = t/(t+d) \leqq 0.72$

where t is a thickness of the first semiconductor layer, and d is a thickness of the second semiconductor layer; and

wherein assuming that a breakdown voltage is represented by VB (V), then t, VB (V), and A satisfy a relationship below:

$t < 2.53 \times 10^{-6} \times (A \times VB)^{7/6}$ (cm),

wherein the first to fifth semiconductor layers are constituted by a silicon layer,

wherein a void is present in a border region between the second semiconductor layer and the third semiconductor layer.

Claim 32 (Previously Presented): A semiconductor device according to claim 31, wherein, assuming that an aspect ratio B is represented by B = d/w, where w is an interval between adjacent third semiconductor layers, the layer thickness ratio A and the aspect ratio B satisfy an expression below:

$$A \times B \leqq 1.15.$$

Claim 33 (Previously Presented): A semiconductor device according to claim 31, wherein an aspect ratio B and the layer thickness ratio A satisfy an expression below:

$$-0.04B + 0.48 < (A \times B) < 0.13B + 0.59$$

where the aspect ratio B is represented by B = d/w, and w is an interval between adjacent third semiconductor layers.

Claim 34 (Previously Presented): A semiconductor device according to claim 31, wherein a product of A × B satisfies a relationship below:

$$0.58 < (A \times B) < 0.71$$

wherein B denotes the an aspect ratio represented by B = d/w, where w is an interval between adjacent third semiconductor layers.

Claim 35 (Previously Presented): A semiconductor device according to claim 33, wherein, assuming that an impurity concentration of the first semiconductor layer is represented by Nn and that a breakdown voltage is represented by VB (V), then Nn, VB (V), and A satisfy the relationship below:

$$Nn > 1.11 \times 10^{18} \times (A \times VB)^{-4/3} \ (cm^{-3}).$$

Claim 36 (Previously Presented): A semiconductor device according to claim 31, wherein an insulating material is interposed between the second semiconductor layer and the third semiconductor layer.

Claim 37 (Previously Presented): A semiconductor device according to claim 36, wherein a void is present in said insulating material.

Claim 38 (Previously Presented): A semiconductor device according to claim 31, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 39 (Previously Presented): A semiconductor device according to claim 32, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 40 (Previously Presented): A semiconductor device according to claim 33, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 41 (Previously Presented): A semiconductor device according to claim 34, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 42 (Previously Presented): A semiconductor device according to claim 35, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 43 (Previously Presented): A semiconductor device according to claim 36, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 44 (Previously Presented): A semiconductor device according to claim 37, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 45 (Previously Presented): A semiconductor device according to claim 31, wherein a plurality of voids are present independently along the border region.

Claim 46 (Previously Presented): A semiconductor device according to claim 31, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 47 (Previously Presented): A semiconductor device according to claim 45, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 48 (Previously Presented): A semiconductor device according to claim 36, wherein, assuming that an aspect ratio B is represented by $B = d/w$, where w is an interval

between adjacent third semiconductor layers, the layer thickness ratio A and the aspect ratio B satisfy an expression below:

$$A \times B \leqq 1.15.$$